LEVEL

SUBMICRON FETs USING MOLECULAR BEAM EPITAXY

ANNUAL REPORT NO. 1

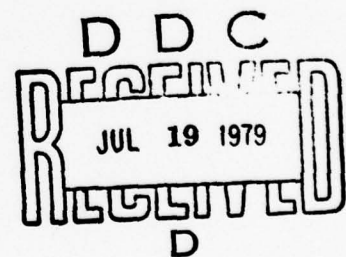(August 1977 - August 1978)

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Electron-beam exposure and MBE material have been used to achieve quarter-micron gate length GaAs FETs. A noise figure of 2.2 dB with an associated gain of 12 dB has been measured at 8 GHz.

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SUMMARY

Using electron-beam exposure and MBE GaAs, FETs have
been fabricated with gate lengths ranging from 0.15 to 0.45
microns. An anodic thinning procedure was developed to remove
the n^+ layer in the gate region, resulting in low source
resistance (3.1 ohms) and high transconductance (30-32 mmhos)
for 150-micron wide devices. A noise figure of 2.2 dB with
an associated gain of 12 dB has been measured at 8 GHz.
Problems with gate resistance, anodization damage, and layer
profiling remain to be solved.

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SYMBOLS

a	Channel thickness
AES	Auger electron spectroscopy
b_{11}	Imaginary part of the FET small-signal admittance parameter y_{11}
C_{gd}	Drain-to-gate feedback capacitance
C-V	Capacitance-voltage
CVD	Chemical vapor deposition
E	Electric field
f	Frequency
FET	Field-effect transistor
g_m	FET transconductance
g_{11}	Real part of the FET small-signal admittance parameter y_{11}
G_a	Associated gain
I_d	FET drain current
L	FET gate length
LPE	Liquid-phase epitaxy
MAG	Maximum available gain
MBE	Molecular-beam epitaxy
n	Electron concentration
N_D	Channel doping
NF_m	Minimum noise figure
PMMA	Polymethyl methacrylate
r_c	FET small-signal channel resistance

r_g	FET gate resistance
r_{in}	FET input resistance
R_s	FET source resistance
SEM	Scanning electron microscope
t	Thickness
T	Temperature
v	Electron velocity
v_s	Saturated electron velocity
V_g	FET gate voltage
VPE	Vapor-phase epitaxy
Z	FET gate width
μ_o	Low-field mobility
ϕ_B	FET gate built-in voltage
ω	Radian frequency

1. INTRODUCTION

"Transient velocity overshoot" was proposed by Ruch[1] in 1972 to partially explain why GaAs, while having only a marginal advantage over Si with regards to the saturated drift velocity in the high field region (Fig. 1) is able to outperform Si in a FET structure. Cold electrons injected at the source may never reach their steady-state velocity before being collected at the drain but travel at a higher velocity, approximately

$$v = \mu_o E \qquad (1.0)$$

where μ_o is the low-field mobility, before relaxation effects take place. This transient phenomenon is due to the disparity between the energy and momentum relaxation times, causing the average velocity in the channel to overshoot its usual saturation value.

Figure 2 shows a computed plot of velocity vs. distance down the channel for both GaAs and InP, assuming a constant field.[2] These plots illustrate the significant role that velocity overshoot can play in increasing the effective electron velocity in sub-micron gate devices. Silicon also shows velocity overshoot, but the improvement is much smaller and would require gate lengths less than 1000 Å to realize it.[1] It may thus be possible to increase the effective saturated velocity in the FET channel without resorting to "super velocity" materials, by reducing the gate length of GaAs FETs.

It may well be that the proposed performance advantages of "super velocity" alloys such as InGaAsP will only be realized by the mechanism of velocity overshoot. As shown
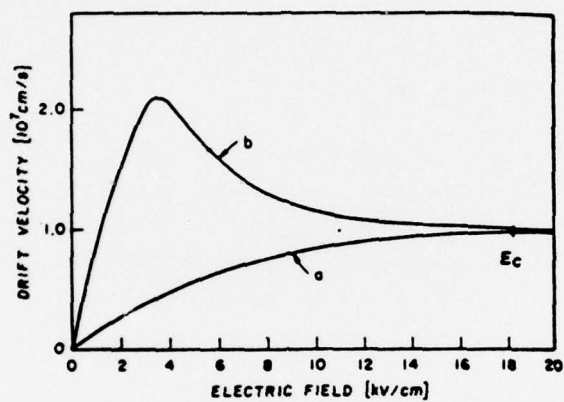
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Fig. 1.   Velocity-field characteristics
           in GaAs and silicon.[1]

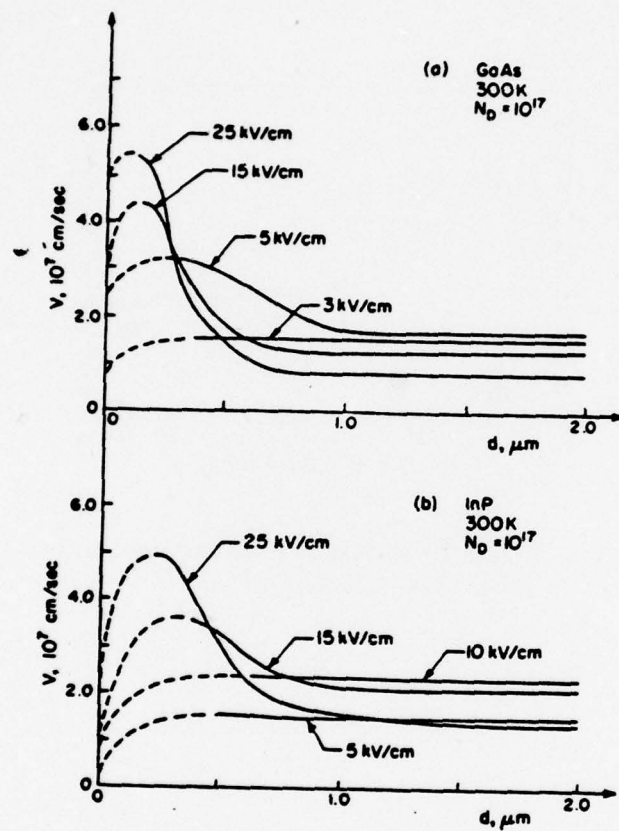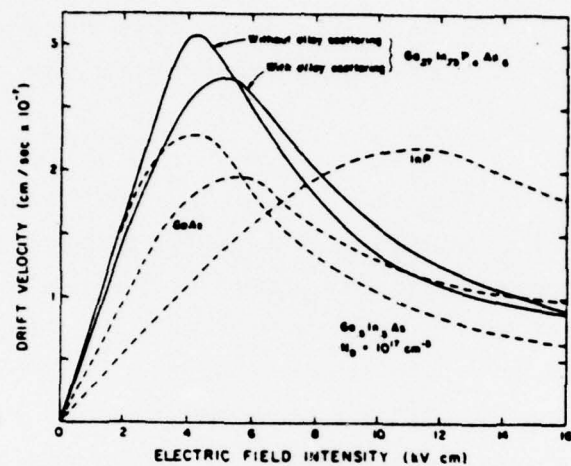Fig. 2. Instantaneous velocity vs distance for 300°K, $N_d = 10^{17}$, (a) GaAs, (b) InP. [2]

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Fig. 3. Velocity-field characteristic of
$Ga_{0.27}In_{0.73}P_{0.4}As_{0.6}$ with and without
random potential alloy scattering. Shown
for comparison are the velocity-field
curves for GaAs, InP, and $Ga_{0.5}In_{0.5}As$. The
doping level is $10^{17}cm-3$.)$_{0.5}In_{0.5}As$. The
doping level is $10^{17}cm-3$.)

by the computations of Littlejohn, et al.[3] in Fig. 3, while the computed static velocity-field characteristic of InGaAsP shows a higher low-field mobility which can be utilized to advantage by velocity overshoot according to Eq. (1), the velocity in the high-field region is less than that of GaAs. Thus, the investigation of the transient effects of velocity overshoot for other materials such as InP, InGaAs, InGaAsP, and other promising materials is also a matter of importance.

Besides the ability to provide quarter-micron openings in resist with electron beam photolithography, the gate metallization scheme must preserve the resist profile, the active layer must be thinner to prevent g_m reduction, and the effective source-gate spacing must be reduced to avoid source resistance domination. In addition to all this, it may be that a reduction in device width or the addition of multiple gate pads may be necessary to overcome the increased gate resistance brought about by using such small gate lengths. If a narrower-width device is used, it may be that a driver FET of larger dimensions must be integrated on the same chip to drive the off-the-chip parasitics involved in the realization of practical broadband microwave amplifiers (being the second stage, its gain and noise figure are of less importance.

2. QUARTER-MICRON GATE FABRICATION

The technique of etching 0.25-micron gates by undercut-
ting a resist mask as is done in fabricating 0.5-micron gate
lengths in our labs was deemed unfeasible. As the gate length
decreases, it is necessary to at least maintain the metal
thickness to avoid gate resistance problems, and to etch
through 4000 Å of Al with 7000 Å of undercutting would mean
that a 1.65-micron line would have to be etched to a uniform
length of 0.25 micron. This has been tried, but most of the
gates were discontinuous and the few that were not were so
ragged that it would be hard to ascribe any particular gate
length to them. The study of velocity overshoot effects
would need to be correlated with a particular uniform gate
length. Consequently, to achieve quarter-micron gate lengths
for this contract, the gate metal was deposited through a
PMMA resist opening defined by electron-beam exposure.

From past experience, the best gate characteristics had
always been obtained with sputtered Pt gates deposited after
a sputter cleaning of the gate area needed to ensure sticking
of the Pt. Gates formed by evaporation of Al followed by a
resist lift-off have frequently shown g_m compression near
zero gate bias. In one case where the gate area was first
sputter cleaned and then trasferred rapidly to another vacuum
system for Al evaporation, no g_m compression was seen.

Using lines exposed in 0.7-0.8 micron thick PMMa resist
by an ETEC Model U-1 Autoscan SEM, it was confirmed that
resist patterns that give 0.15 to 0.2 micron evaporated Au
gate lengths also give 0.35 to 0.4 micron sputtered Pt gate
lengths. These trials were done by exposing the PMMa resist

on the wafer, breaking the wafer in two, and evaporating Au
on one half and sputtering Pt on the other half. Evidently
the sputtering process itself widens the resist both during
the sputter cleaning and during deposition as shown in Fig.
4. Perhaps also the resist has a overhang which would cause
the sputtered gates to be wider than the evaporated gates.
Reducing the sputter voltage from 1000 V to 600 V did not
help, and neither did elimination of the sputter cleaning
step before deposition.

Gates were electron-beam exposed in PMMA resist and
developed. It appeared that the developed resist walls were
near to being vertical when observed with the SEM (hopefully
with the intensity low enough so as to avoid altering the
resist profile while in the act of looking at it). The
wafer was then halved and one half was dc sputter cleaned
for 10 min at 1 keV in argon. 1600 Å of Au was then evaporated
on both halves and lift-off was used to form the gates. It
appeared that the sputter-cleaned gates were around 0.05 to
0.1 micron longer than the unsputtered-cleaned gates. This
would indicate that the sputtering process itself widens the
resist opening apart from any widening that might occur due
to the ability of sputtered material to deposti under an
overhang in the resist.

Narrowing the resist lines below 0.15 micron so that
after sputtering the gates would be 0.25 micron would be
difficult without using thinner resist. The resist thickness
must be kept at 0.7 to 0.8 micron to obtain good liftoff of
the 4000 Å gate metal thickness (needed to maintain low gate
resistance for such narrow gates). Sputtering may not be
the way to go anyway for the additional reason that the
sputter cleaning always non-uniformly removes some material,
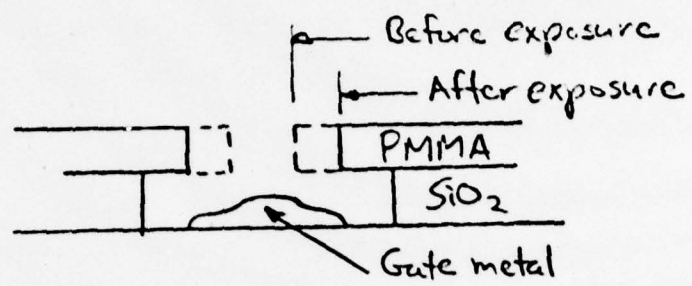and this could be a problem for thin channel devices.

Fig. 4. Resist recession.

An effort was made to evaporate Pt using a new 6-kW
E-gun system.   1000 Å of Pt was put down at 1.3 kW, followed
by 3000 Å of Au at ~0.5 kW. Evidently the Pt evaporation
was too hot for the PMMA, causing the resist to recede from
its original profile as shown in Fig. 4 to give an approximately
0.4-micron long gate. Evaporation of W was also tried with
the same system, and the heat generated actually fried the
resist.

Using evaporated Al, quarter-micron gates could be easily
obtained, but Al has been found to give g_m compression near
zero gate bias, as has previously been mentioned. The decision
was thus made to use evaporated Au as the gate metal in light
of all the aforementioned problems with other metallization
schemes. Although the use of Au does not give a reliable
gate because of possible interaction with the underlying
GaAs with time and temperature, it should be adequate for
the purposes of studying performance and velocity overshoot
immediately after device fabrication. Au does not stick
well to GaAs, so special precautions were taken to ease the
liftoff procedure by using a 1000 Å SiO_2 layer under the
resist as shown in Fig. 4 and avoiding the use of ultrasonic
energy.

Figure 5 shows the gate for one of the devices fabricated
on a part of an InGaAs wafer used for InGaAs run #59 (8.5% In)
on ONR Contract N00014-75-C-0125.[4]   The evaporated Au gate
length is only 0.15 micron, with the device being fabricated
as part of the study mentioned previously to determine the
effects of sputter cleaning on the gate length. Only half
the gate was intact because of poor Au adhesion. Figure 6
shows the drain characteristic for half of the device
(Z = 75 microns), revealing fairly good saturation with no
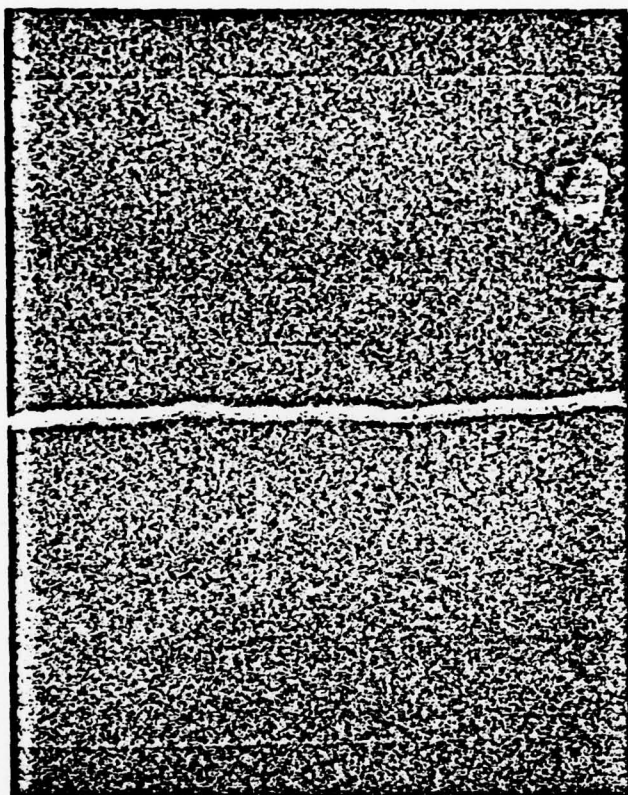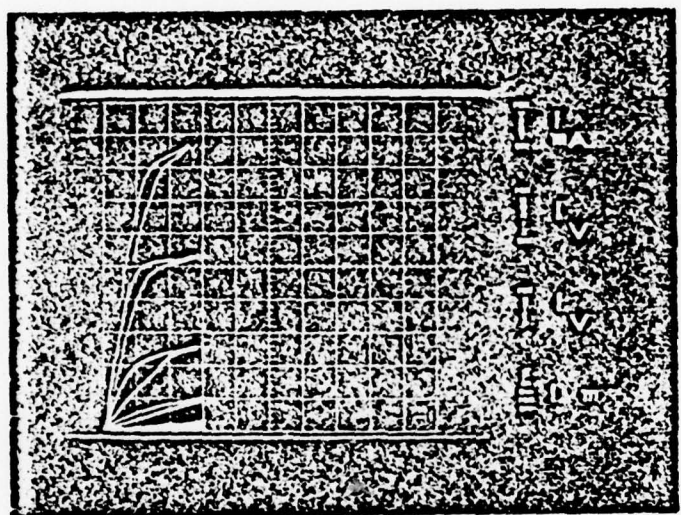g_m compression at zero gate bias.

Fig. 5. 0.15 micron gate (1.688 x 10^4 mag.)

half of a device by 2 i 14kjem hx yte 86v i

Fig. 6 . Drain characteristic of Fig. 5 device.

Figure 7 shows a plot of I_d vs. gate gias for device
#59-1 (L = 0.74 micron) and for the Fig. 6 device (multi-
plied by a factor of two to simulate a whole device for
purposes of comparison). I_d at zero bias is a little lower
for the Fig. 6 device, probably because the active layer is
a little thinner in this portion of the wafer. In spite
of the lower current, it is significant to note that the
pinch-off voltage is about a volt higher! This would seem
to be an indication of the effect described in Ref. 5 where
because the gate length is less than the channel thickness,
the gate depletion layer is circular instead of flat, requiring
more voltage to deplete to the same depth and thus reducing
g_m. The channel thickness is around 0.2 to 0.25-micron thick
with a doping of $10^{17} cm^{-3}$. The solution to this is to increase
the channel doping to around 2-4 x $10^{17} cm^{-3}$ and decrease
the thickness, which suggests the use of MBE for better
control of thin growth. The problem will also be alleviated
by going to 0.25-micron gate lengths.

$I_{DS}(mA)$

$L_g = 0.74$ micron

$L_g = 0.15$ micron

30

20

10

00

13

-1

-2

-3

-4

Fig. 7. Long and short gate comparison.
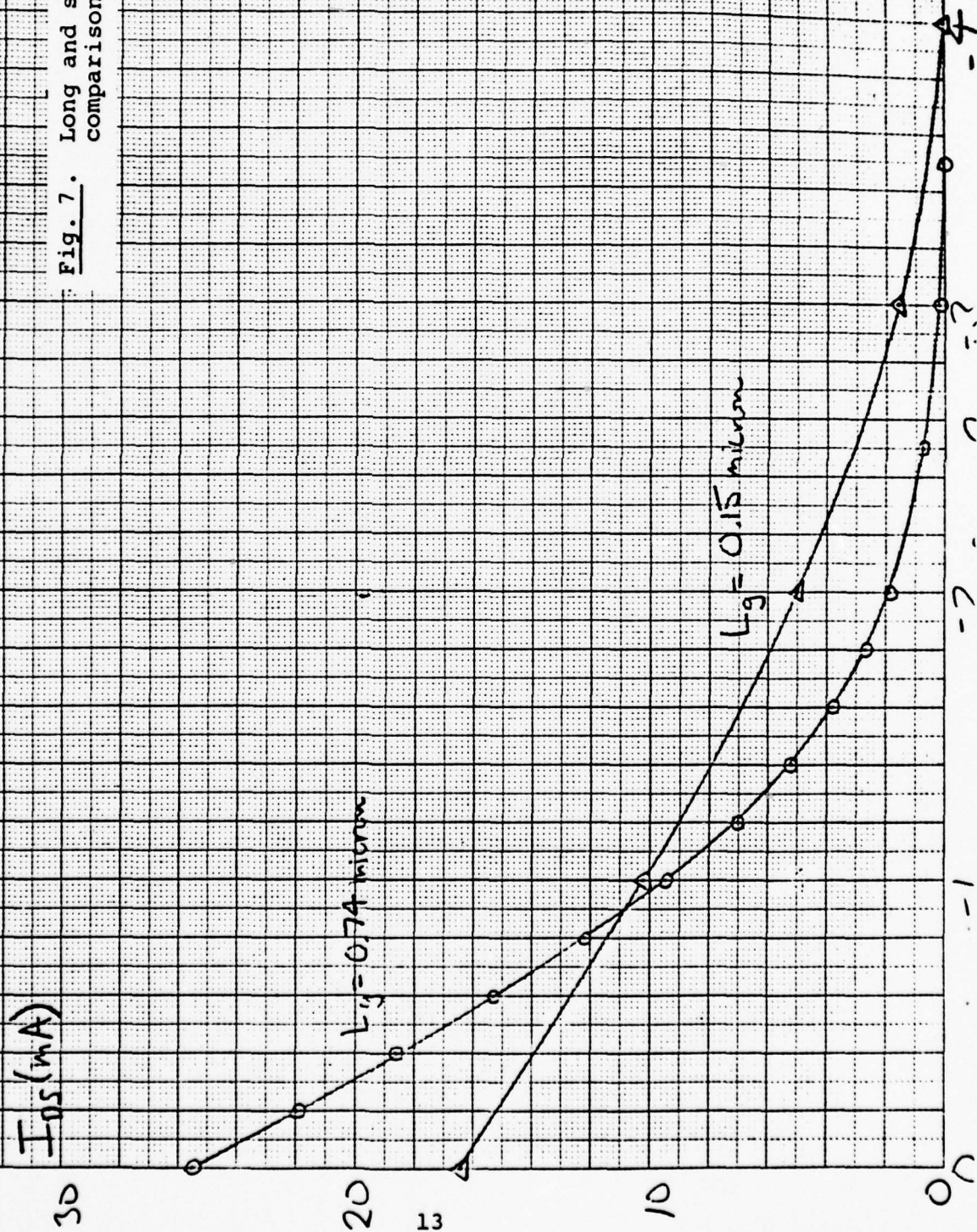
3.   GROWTH OF EPITAXIAL LAYERS FOR LOW NOISE FETs BY MBE

The growth of epitaxial layers of Sn-doped GaAs by MBE
for the fabrication of low-noise FETs has been developed to
the stage where layers of desired thickness and donor concen-
tration can be routinely and reproducibly grown. The epitaxial
structure for the FETs described in this report consists of
an undoped GaAs buffer layer (~1-2 microns thick) grown on
a Cr-doped GaAs substrate followed by an active layer with
$n \approx 3.5 \times 10^{17} cm^{-3}$ (~1200 Å thick) and finally a contact layer
with $n^+ \approx 2.5 \times 10^{18} cm^{-3}$ (~1000 Å thick).

In order to grow this structure by MBE, it was first
necessary to grow device quality n-type GaAs by MBE. This
was accomplished using Sn as the donor impurity. For
$n \geq 10^{16} cm^{-3}$ the mobilities of Sn-doped MBE GaAs grown in
this laboratory are comparable to n-type GaAs grown by LPE
and VPE techniques (see Fig. 8).

To evaluate the effective saturated velocity of the MBE
material, 150-micron wide FETs having a gate length of 0.5
micron were fabricated on $10^{17} cm^{-3}$ material grown atop a one-
micron undoped buffer layer. Figure 9 shows a plot of the
drain current I_d vs. $\sqrt{\phi_B - V_g + I_d R_s}$ whose slope is proportioned
to the saturated drift velocity V_s at the gate depletion region
edge. The linearity of the plot from zero gate bias to pinch-
off shows that there is no velocity degradation at the interface.
A value of around $1.3 \times 10^7 cm/sec$ was obtained for v_s from the
slope, which is typical of the values obtained from devices
having similar gate lengths fabricated on VPE grown layers.
A minimum noise figure of 2.5 dB with an associated gain of
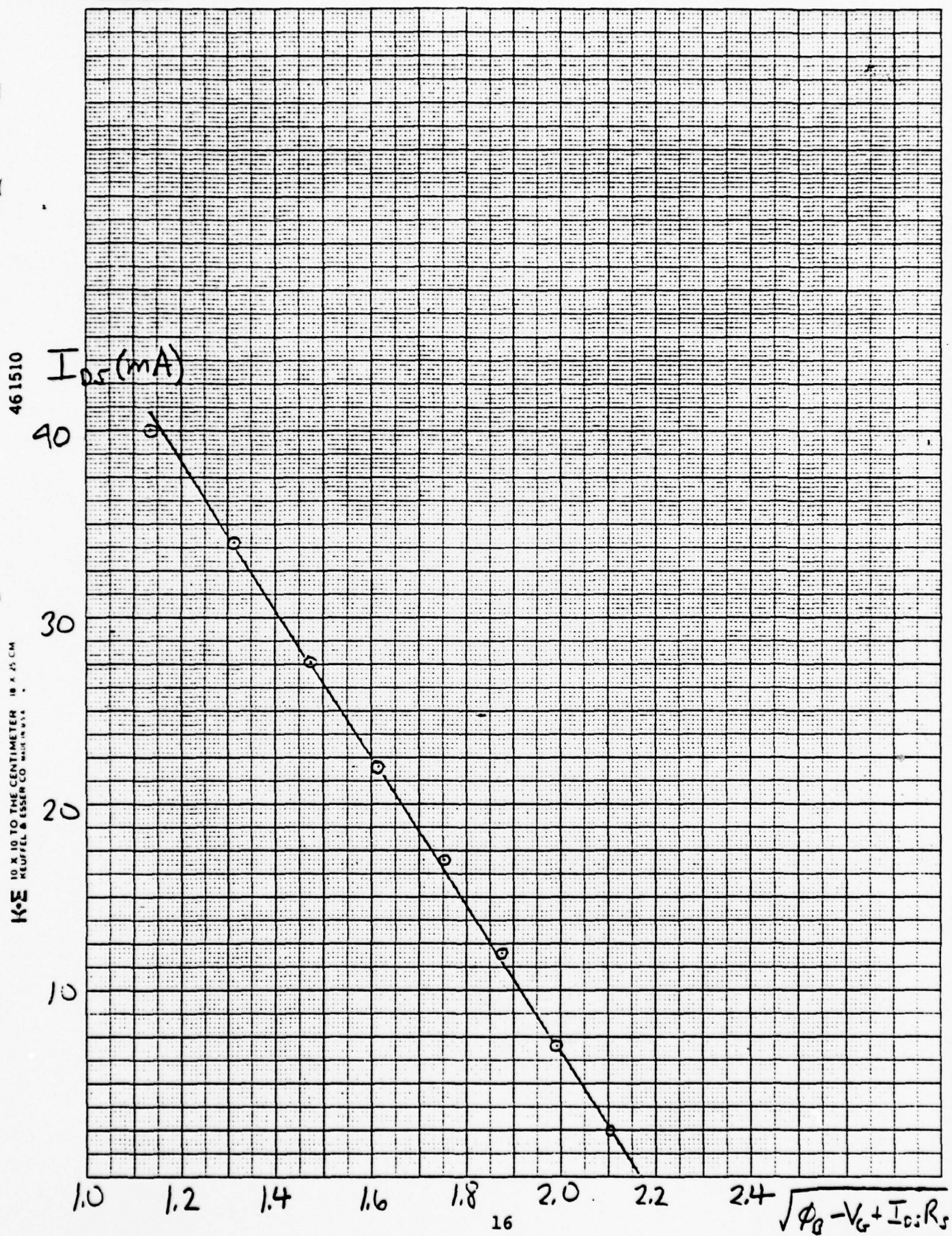9.4 dB was obtained at 8 GHz from these devices.

After demonstrating the ability to grow device quality
n-type GaAs by MBE, it was necessary to develop growth procedures
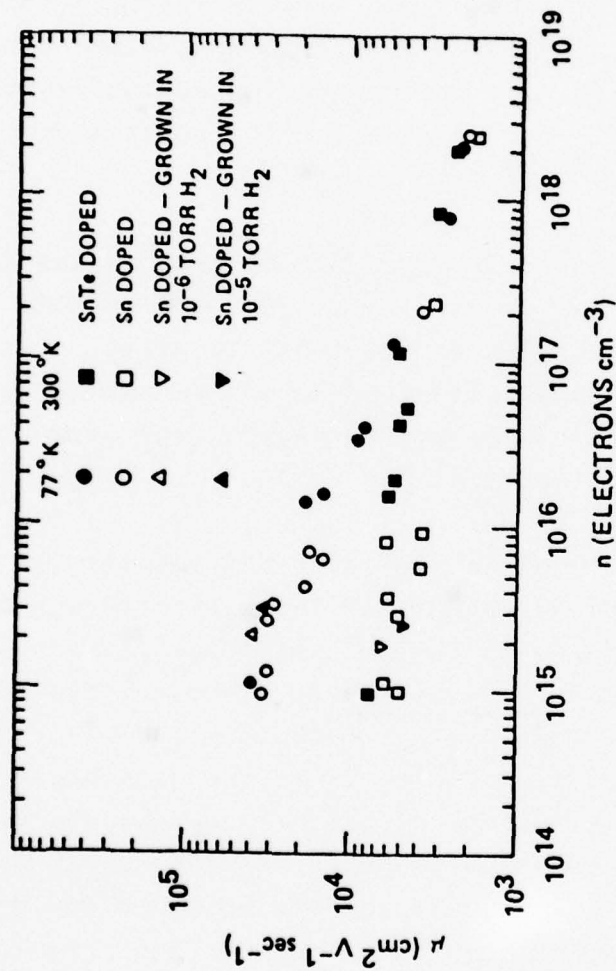
Electron mobilities versus doping for n-type MBE GaAs.

Fig. 8

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Fig. 3. Saturated drift velocity determination for MBE growth.

Fig. 3. Saturated drift velocity determination for MBE growth.

which overcome the problems resulting from Sn segregation
at the surface of the film during MBE growth. This Sn
segregation results in non-abrupt changes in donor concen-
tration and hence doping profiles which are not suitable for
FETs. To overcome this problem, a procedure involving pre-
deposition of Sn prior to initiating growth was developed.

The problem imposed on obtaining abrupt doping transitions
due to Sn segregation is illustrated in the C-V profile of an
FET active layer shown in curve #1 of Fig. 10. The target
values for doping and thickness of this layer were $n = 10^{17} cm^{-3}$
and $t = 0.3$ micron, respectively. The layer was grown at
$T_{substrate} = 544°C$ following a 15-minute Sn predeposition
which was intended to negate the effects of Sn segregation.
The lack of a sharp step change in doping concentration in
this C-V profile clearly indicates that the 15-minute Sn
predeposition was not adequate.

Figure 11 displays the results of Auger electron spectro-
scopy (AES) measurements of Sn segregation carried out for
$T_{substrate} = 581°C$ and $T_{Sn\ furnace} = 981°C$ (corresponding to
a steady-state donor concentration of ~2.5 x $10^{18} cm^{-3}$ as
measured by Van der Pauw). Based on the relative intensity
of the Sn 450 eV Auger transition with respect to the low
energy (0-100 eV) As and Ga Auger transitions, the 60-minute
Sn predeposition resulted in approximately a full monolayer
of Sn on the GaAs surface (Fig. 12).

After a total of 60 minutes of Sn predeposition, a 1.35-
micron thick epitaxial layer was grown under the same conditions
as those used for the Sn predeposition (i.e., $T_{substrate} = 581°C$,
and $T_{Sn\ furnace} = 981°C$). After this growth, AES indicated
that the same concentration of Sn was present on the GaAs
surface as that present after the 45-minute Sn predeposition.
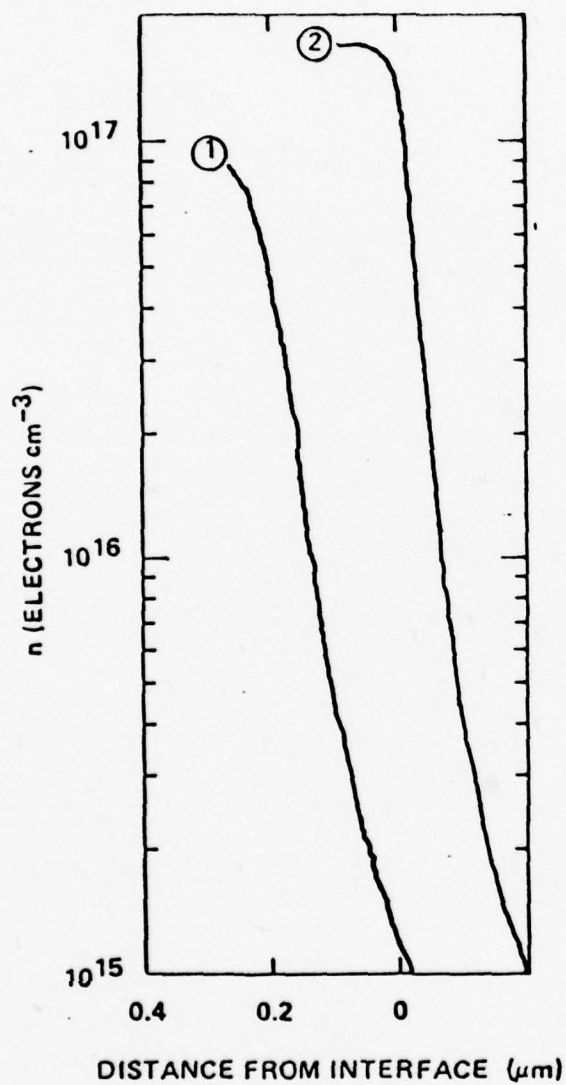
Doping profiles for two different MBE GaAs films.

(1)   Sn doped, $T_{substrate}$ = 544 °C, 15 minute Sn predeposition.

(2)   Sn doped, $T_{substrate}$ = 581 °C, 45 minute Sn predeposition.

<u>Fig. 10</u>.   18

The graph shows handwritten annotations:

$T_{Sn\ furnace} = 981\ °C$

$\Rightarrow n_{steady-state} \approx 2.5 \times 10^{18}\ cm^{-3}$

$T_S = 581\ °C$

Y-axis: Intensity of Sn 430eV Auger Transition (arbitrary units)

X-axis: Sn Predeposition Time (min.) — 15, 30, 45, 60
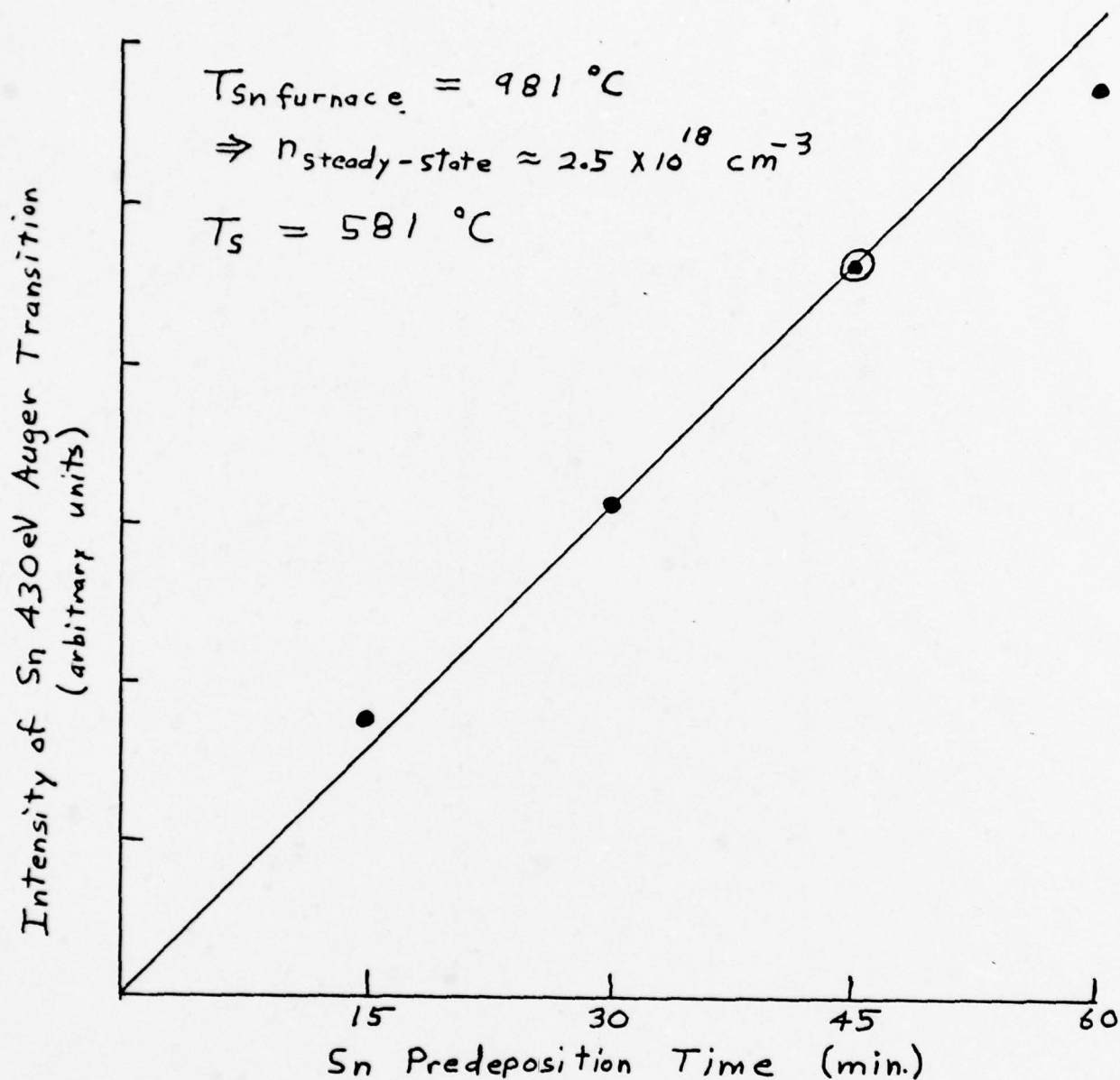
The circle at t = 45 min. indicates the intensity of the
Sn 430 eV Auger transition after a 1.35 μm epitaxial growth
following the 60 min. Sn predeposition. This indicates that
for $T_{Sn\ Furnace}$ = 981°C and $T_{Substrate}$ = 581°C a 45 min. Sn
predeposition is necessary to obtain an abrupt change in doping.
The steady-state doping under these conditions is n = 2.5 X 10^{18} cm^{-3}.

Fig. 11.   19
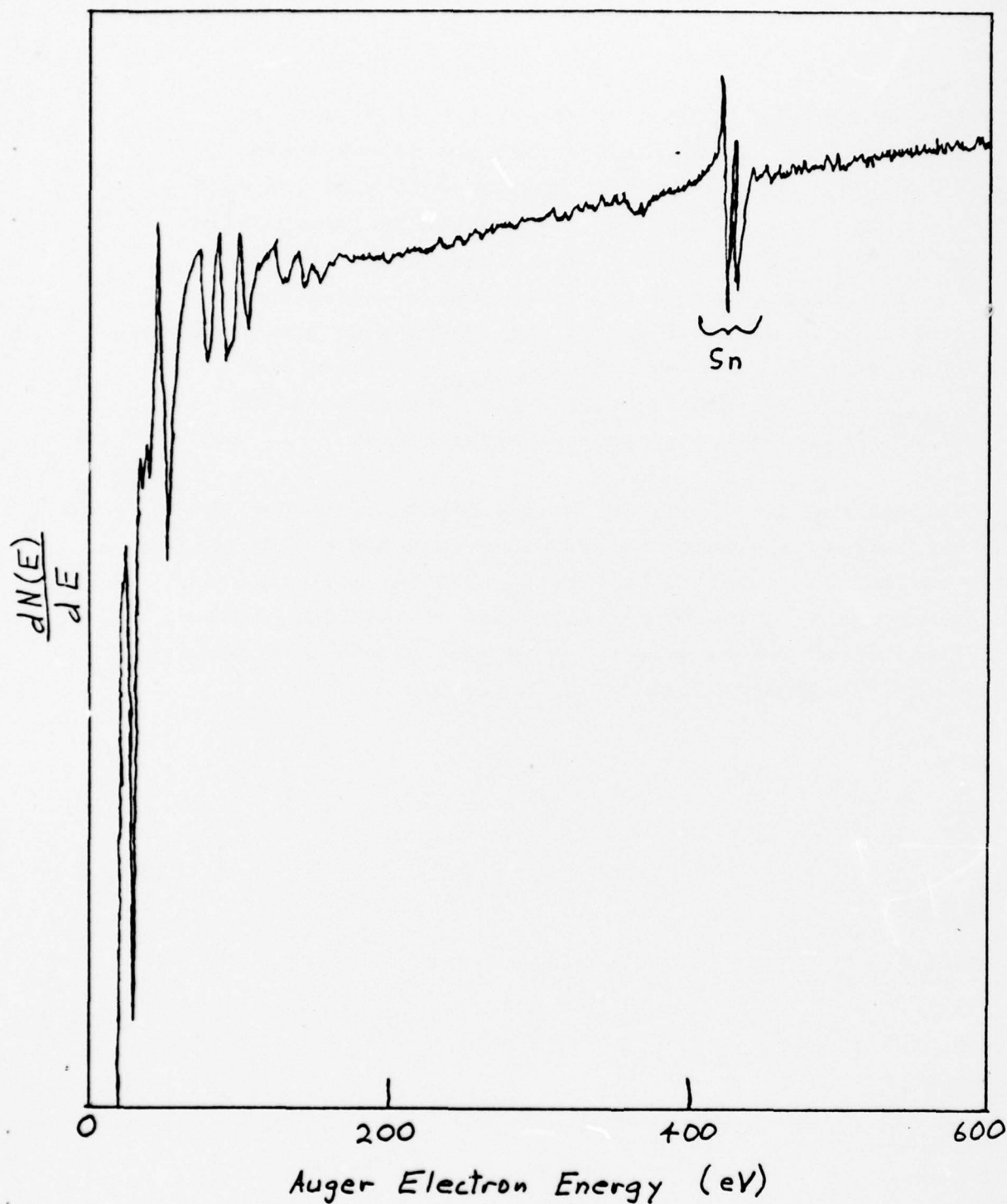
Auger spectrum of GaAs substrate after 60 min. Sn predeposition with $T_{Sn\ Furnace} = 981°C$ (corresponding to a steady-state donor concentration of $2.5 \times 10^{18}\ cm^{-3}$) and $T_{Substrate} = 581°C$.

Fig. 12.   20

This is indicated by an open circle at t = 45 minutes in Fig. 11. Since it can be assumed that the steady-state doping level had been reached by the completion of the 1.35-micron growth, it is clear that a 45-minute Sn predeposition is required to achieve a sharp doping transition under the conditions of this experiment. That this is indeed the case is illustrated in curve #2 of Fig. 10, where a Sn predeposition time of 45 minutes was used with $T_{substrate}$ = 581°C and $T_{Sn\ furnace}$ = 876°C (steady-state donor concentration of $2 \times 10^{17} cm^{-3}$ based on Van der Pauw measurements).

Through the use of this Sn predeposition technique at both the buffer layer-active layer interface and at the active layer-contact layer interface, the n^+-on-n FET structure has been successfully grown by MBE. Because of the high degree of control which can be achieved with MBE, it has been possible to routinely reproduce this device structure.

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4. DEVICE FABRICATION AND EVALUATION

The device geometry used on this phase of the contract is that used for the 0.5-micron self-aligned FETs produced by Varian (Fig. 13), with the only difference being that the gate is written as a straight line with the ETEC Autoscan SEM controlled by a VDM 620/i minicomputer. The SEM also writes the 1.5-micron wide leg connecting the gate to the gate pad. Alignment of the gate is accomplished by aligning two points on the SEM CRT which define the gate trajectory with respect to the outermost edges of the source. The remainder of the processing for this 150-micron-wide device is with conventional photolithography.

4.1 Anodic Thinning of the Channel to Lower R_s

It was determined that the gate could not be aligned in the SEM closer to the source than about 0.5 micron. The beam is focused on a device mesa (which destroys the device) after which about five gate exposures are done before refocusing the beam again. Movement of the stage to expose a new device causes the beam to in general go slightly out of focus, thus changing the gate length and perhaps altering where the gate is written with respect to its intended position as indicated by the alignment marks. Additionally, the source edge is shifted by an amount in crossing the mesa edge (Fig. 14), and this amount cannot be determined from the narrow window slits used for alignment. Furthermore, as shown in Fig. 15, the source edge is not well-defined, perhaps because of using a combination of evaporation and sputtering to deposit it. And finally, the source metallization is around 6000-7000 Å thick so that the resist is thicker near the source as shown in Fig. 16, resulting in poor gate exposure if done too near the source.

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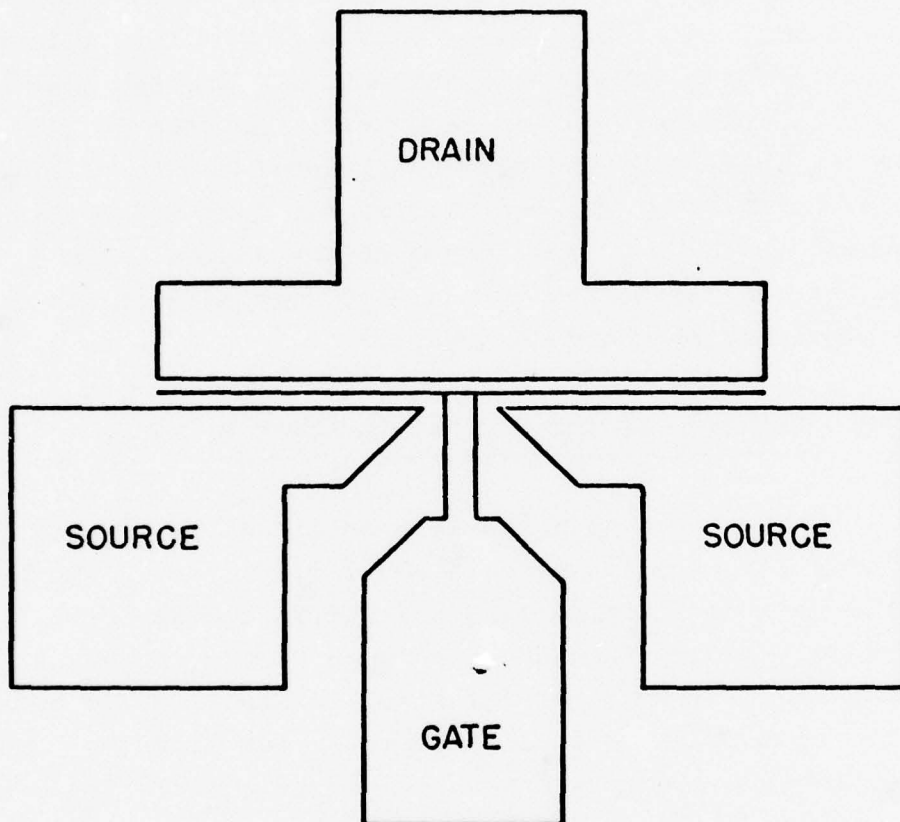
Fig. 13. FET geometry used for electron-beam exposed gates.

ALIGNMENT WINDOW
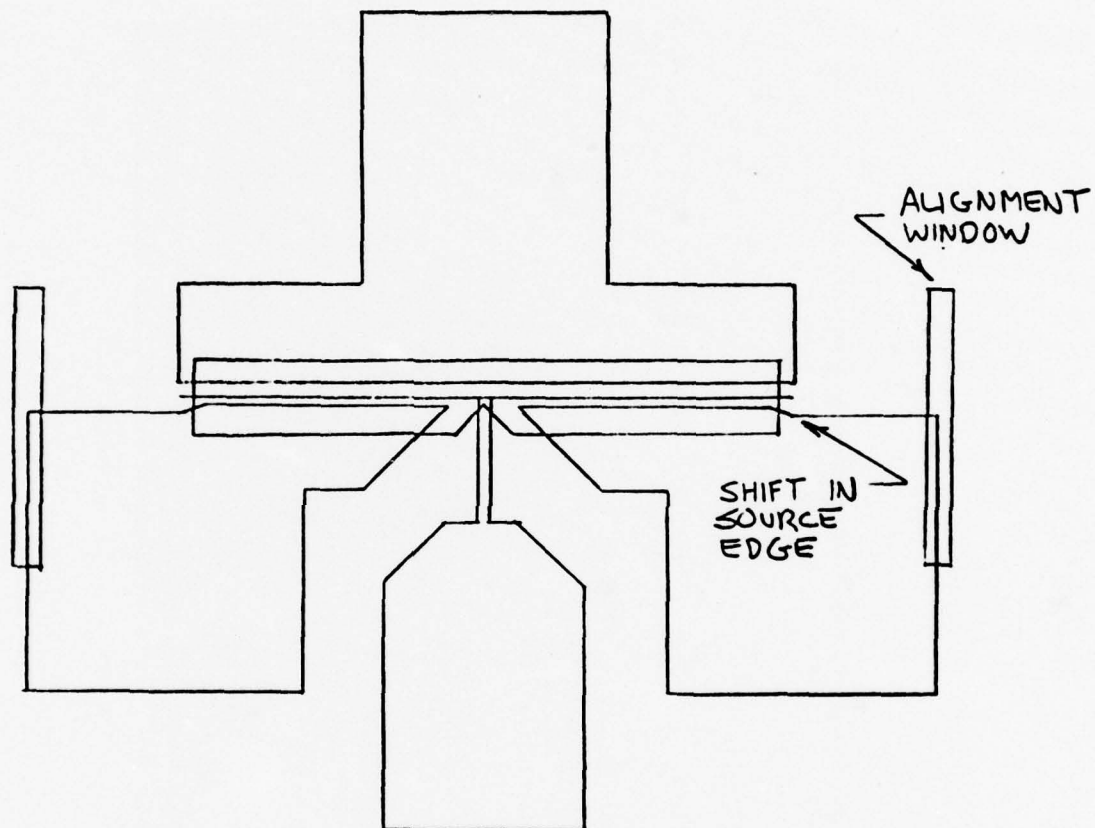
SHIFT IN SOURCE EDGE

Fig. 14. Source edge shift over mesa.
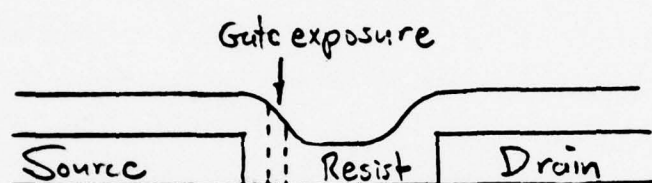
Fig. 15. Ill-defined source edge.

25

Fig. 16.   Thick resist near the source
preventing good edge exposure
when the gate is placed near
the source.

A source-gate spacing larger than the gate length would mean parasitic dominance of the small signal parameters. Source resistance would dominate the channel resistance, r_c, in determining g_{11}, resulting in a loss of gain and a higher noise figure unless the gate resistance dominates both r_c and R_s.

Figure 17 gives the process that was developed on this contract to provide a self-aligned technique for minimizing the source resistance. The n^+ layer will lower the contact resistance of the source contact and enable the "effective" source-gate spacing to be on the order of 0.1 micron or less. Figure 17(e) shows that thicker gate metal can be lifted. It was originally hoped that the freshly-etched gate trough would enable Al to be evaporated without the accompanying g_m bunching, but such was not the case. The very thin channel needed for a small gate length (in addition to the sensitivity of the etch rate to slight variations in the resist opening) precludes using ordinary solution etching. Anodic thinning enables good control of the channel thickness to be achieved, independent of etch rate variations from device to device, and lateral etching can be achieved to avoid contact of the gate with the n^+ layers without affecting the channel thickness.

MBE is especially suited for growing the n^+ layer because of its lower growth temperature and its ability to abruptly increase the doping significantly with the wafer remaining in-situ. The VPE systems in operation use Sn and S as n-type dopants. The Sn source is molten and is capable of only a factor of around three in doping change, while efforts using S have revealed that the n^+ layer diffuses into the thin active layer so that there is little, if any, thickness of constant-doped active layer.

(a) Starting material

n+
n
Semi-insulating buffer
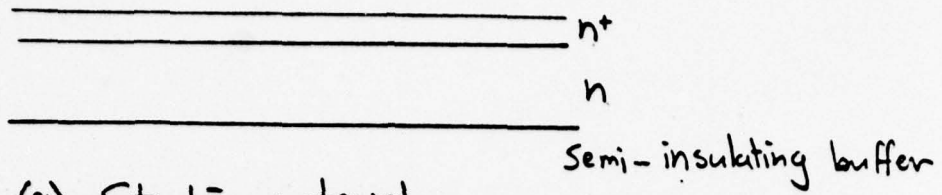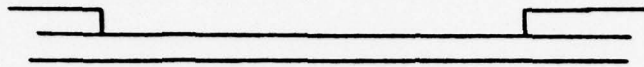
(b) Ohmic contacts

(c) Gate definition

PMMA   SiO₂
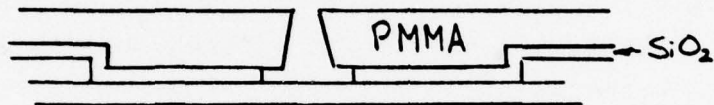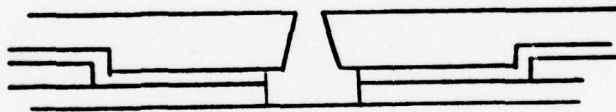
(d) Anodic etch

(e) Gate deposition

Fig. 17. Gate anodization process.

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Using molecular beam epitaxy, 1500 Å of GaAs doped $2 \times 10^{17} cm^{-3}$ followed by 500 Å of greater than $10^{18} cm^{-3}$ doping were grown on a Cr-doped semi-insulating substrate. Because of the n^{+} layer, no doping profiles could be taken, so that the parameters listed are only estimates. Without forming mesas (so that electrical contact could be made to each device via tweezers) source and drain ohmic contacts were put down, followed by PMMA spin-on and gate exposure. The channel was anodically thinned using phosphoric acid diluted with water to a pH of 2.8. With 18.6 Å/V[6] and using 50 V to increase the amount of GaAs removed and to make the oxide visible resulted in the resist lifting and the Au-Ge/Ni ohmic contacts being severely attacked. Even voltages as low as 6V were found to attack the ohmic contacts, albeit not so vigorously (in exposing the gate pattern with the SEM, alignment using the ohmic contacts always bares a portion of the metal). As the anodic voltage is increased, the attack on the ohmic contacts increases and extends further under the resist until at 50 V almost all of the ohmic contact is destroyed (as shown in Fig. 18) in the time it takes to grow the oxide.

While the lower voltages did not cause any observed resist lifting, the resist was found to lift at 25 V which is about the lowest voltage that can be used and yet see the oxide. Deciding to solve the resist lifting first, 500 Å of SiO_2 was CVD deposited over an unmetallized wafer. The PMMA resist was then spun over it and exposed and developed, followed by an SiO_2 etch and the anodization. The thinking was that the resist was lifting because it too was being anodized at the GaAs-resist interface, and an insulating layer between the resist and the GaAs should prevent this. The scheme worked, and Fig. 19 shows a photo of the results after a 50-V anodization and gate evaporation.
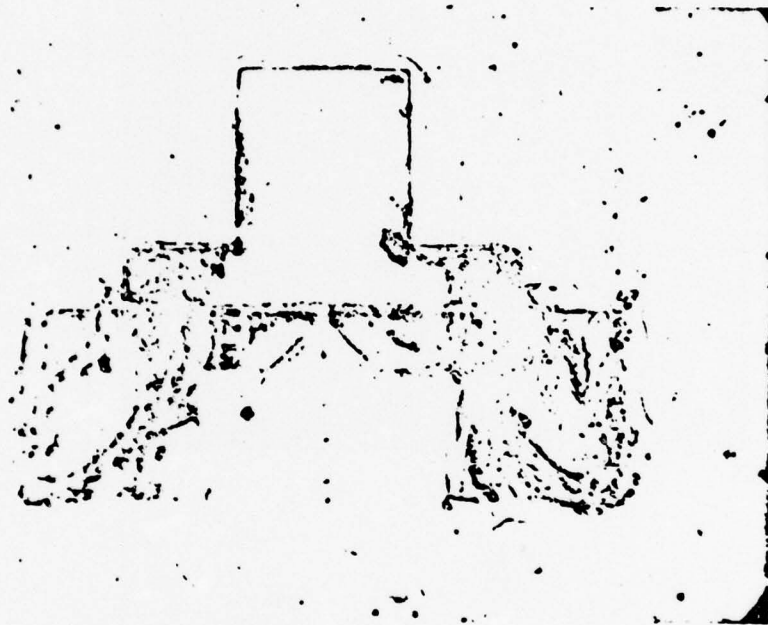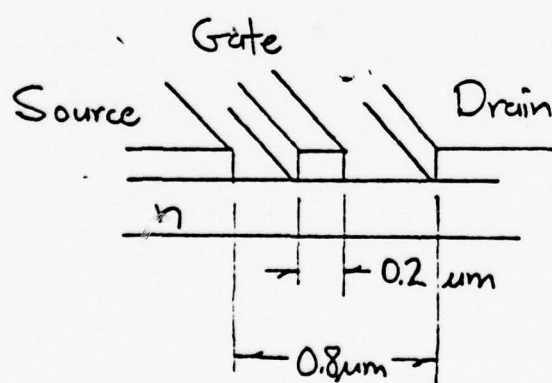
Fig. 18. Anodic attack of
the ohmic contacts.

Fig. 19. Anodically thinned
channel and gate.

When the ohmic contacts were employed, the SiO_2 did not
prevent the attack of the metallization from spreading outward
from the areas bared by the alignment. Under the hypothesis
that this was because of poor adhesion of the SiO_2 to Au, an
Al layer was put over the Au to promote the SiO_2 adhesion.
This stopped the attack on the metallization except in the
small exposed areas resulting from alignment. However, Al
on Au is unacceptable for well-known metallurgical reasons
(it was used for a quick method of determining if better
adhesion would solve the problem, which it did). The Al
could be etched off afterwards, but if the gate were Al it
would be removed also. A layer of Ti-W was tried over the Au
and worked fairly well, although not as well as the Al. The
Ti-W would also serve the purpose of acting as a barrier
between the ohmic contact and the Au overlay, improving both
the contact resistance and the bondability.[7] The adhesion
of SiO_2 to W was mediocre, but certainly better than the SiO_2
to Au. How much the Ti helps is not certain since it is present
only in a 10%-alloy form with the W, and the HF used to remove
the SiO_2 used in defining the ohmic contact patterns also
attacks Ti. A subsequent deposition of more Ti-W followed
by Au after the anodization was found to provide a very good
surface to bond to.

During the course of the anodization studies, an inter-
esting phenomenon was observed. Whereas the anodic thinning
of the wafer would stop when the breakdown voltage equaled
the pinch-off voltage when the whole wafer surface was being
anodized, when anodically thinning the thin gate regions the
oxide growth would continue indefinitely unless it was abso-
lutely dark and removed when done (it would still continue
slowly even in the dark). Evidently this is because of the
concentration of the thermally-generated holes when etching

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a thin region in contrast to the whole wafer surface. For
actual device fabrication, light was used along with a
determined voltage to remove a given amount of material, so
this phenomenon was of little concern.

The procedure used for the ohmic contacts was evaporation
of Au-Ge/Ni/Au followed by ~700 Å of sputtered Ti-W and ~100 Å
of Ti to promote oxide adhesion. After anodization, another
700 Å of Ti-W was sputtered followed by an evaporated Au
overlay.

4.2 Device Evaluation

Aluminum was evaporated onto a Cr-doped substrate and
lifted to form patterns for determining its conductivity.
The Al thickness was 5220 Å and was measured to have a con-
ductivity of 2.66×10^{-6} ohm-cm, i.e., bulk conductivity.
Hence, for an 0.25-micron long gate, the gate resistance
should be 2.7 ohms using Eq. (B5b) of Wolfe.[8] The wafer
was then alloyed at 455°C for 15 sec without any deterioration
of the conductivity: It appears that the gates can be singed
without altering the conductivity of the metallization.

Following development of anodic thinning in the gate
region to the point of being applicable to actual device
runs, device run EB1 was made on an n^+-on-n MBE wafer (#85).
The n^+ layer was nominally 1000 Å and $\geq 10^{18} cm^{-3}$, and the
n layer was 1500 Å thick and doped $2 \times 10^{17} cm^{-3}$; however,
the high doping of the n^+ layer precludes obtaining a doping
profile. The drains were connected to enable anodization
with mesas, and W-Ti was used for promoting oxide adherence
to the ohmic contact metallization. Al was used for the gate
metallization. Because of difficulty in lifting the gate
pad and the source-drain overlay patterns, ultrasonic energy

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was used which in turn caused all of the gates to break or lift off. Although no complete gated devices were found for which rf data could be obtained, curve tracer measurements indicated that devices having complete gates would have a high g_m of around 30 mmhos. Those portions of the gates that did exist were 0.4 to 0.5 microns long.

A run was made on a wafer having the active layer grown by VPE (doped 3-4 x 10^{17}cm^{-3} and 1100 Å thick as revealed by C-V profiling) followed by an n$^+$ layer grown by MBE (nominally doped $\geq 10^{18}$cm^{-3} and 1000 Å thick). This combination was tried in order to overcome the difficulties associated with growing an n$^+$ layer by VPE (because of S diffusion) and the difficulties of profiling the MBE active layers. Evidently 1000 Å was not enough distance for the Sn to build up to properly dope the n$^+$ layer in spite of an Sn predeposition since the source resistance R_s was a very high 50 ohms.

Run EB3 was made on VPE wafer TR55-9 (no n$^+$ layer, doped 3-4 x 10^{17}cm^{-3} and 1100 Å thick) to simplify the processing and to see how significant the source resistance is in limiting the performance when no n$^+$ layer is used (there was some evidence from Run EB1 that the MBE n$^+$ growth was not reaching 10^{18}cm^{-3}). Run EB2 was made on the same material, but because of the problem depicted in Fig. 16, there was no yield. The gate lengths ranged from 0.25 to 0.5 micron. There was a problem with getting the ohmic contacts to become ohmic after the alloy for some reason, necessitating a repeat of the alloy several times. All of the devices exhibited g_m compression near zero gate bias. Up to and including this run, the Al gates used with anodization had not showed g_m compression while those without it had, seeming to indicate the need for anodic cleaning.

Table I gives the rf data obtained at 8 GHz for some of
the devices from Run EB3 (the pinch-off voltage is around 3 V).

TABLE I

8-GHz Performance for Run EB 3

Device	Maximum Available Gain MAG (dB)	Minimum Noise Figure NF_m (dB)	Associated Gain G_a (dB)	Gate Length L (μm)
EB 3-1	15.2 (V_g = -1.25V)	2.45	10.7 (V_g=-1.89V)	0.4
EB 3-2	13.1 (V_g = -1.82V)	3.54	10.0 (V_g=-2.28V)	0.625
EB 3-9	15.4 (V_g = -1.8 V)	2.71	12.3 (V_g=-2V)	0.39

All the 0.25-micron gate devices were burned out, leaving only
the longer gates for testing. For all of the devices tested,
no oscillations occurred at zero gate bias where the gain was
low due to g_m compression. As the gate bias was increased,
oscillation set in (possibly of the Gunn type) which went
away with further increase in gate bias. Because of the g_m
compression, MAG is not as high as it could be. Furthermore,
it is not certain what effect the phenomenon that causes g_m
compression has on the minimum noise figure NF_m.

Bell Laboratories' formula for NF_m[9] was used to see
whether it could predict the values measured in Table I.
Although the formula appears too rudimentary, it seems to
be able to preduct what they measure within 0.1 dB or less.
The technique of Pucel, et al[10] is in contrast very cumbersome

and prone to calculation errors. According to the BTL
formula, if the parasitic gate and source resistances
(r_g and R_s) are zero, $NF_m = 0$, taking into account none of
the noise arising from the intrinsic device such as intervalley
scattering noise which has been reported to be important.[11]
Including the intrinsic channel resistance, r_c, into the
formula gives

$$NF_m = 1 + KfL^{5/6} \left(\frac{N_D}{a}\right)^{1/6} Z^{1/2} \left(r_c + r_g + R_s\right)^{1/2} \tag{2}$$

where $K = 0.033$ for "good FETs," f is the frequency in GHz,
L the gate length in microns, N_D the channel doping in units
of $10^{16} cm^{-3}$, a the active layer thickness in microns, and Z
the gate width in mm. The transient behavior of velocity
implies a transient behavior of electron temperature as a
function of distance in the channel, which could be expected
to alter the value of K in Eq. (2). At any rate, Eq. (2) will
provide a basis of comparison and will provide a measure of
the effect of the parasitic resistances upon the noise figure.

The assumption will be made that the device input
resistance is given by

$$r_{in} \cong r_c + r_g + R_s \tag{3}$$

Y-parameters were measured at 8 GHz at the appropriate gate
bias for NF_m, and the input resistance r_{in} was then determined
from

$$r_{in} \cong \frac{g_{11}}{g_{11}^2 + \left(b_{11} - \omega C_{gd}\right)^2} \tag{4}$$

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where C_{gd} is the drain-to-gate feedback capacitance. The y-parameter measurements cannot be made on the devices for which the rf data were obtained (since they are mounted in a matched amplifier circuit), and hence were made on two additional devices, EB 3-6 and EB 3-8. Table II summarizes the results.

TABLE II

Computed Noise Figure Performance at 8 GHz for Run EB 3

Device	r_{in}(ohm)	R_s(ohm)	L(μm)	NF_m (dB) Calc.	Meas.
EB 3-6	25	--	0.39	2.07	--
EB 3-8	36	12.4	0.2	1.52	--
EB 3-1	--	10.	0.4	--	2.45
EB 3-2	--	28.4?	0.625	--	3.54
EB 3-9	--	17.2	0.39	--	2.71

The question mark behind R_s for EB 3-2 indicates uncertainty due to the fact that the drain characteristic deteriorated when the device was observed in the SEM for purposes of gate length measurement after the rf measurement but before the R_s measurement. It is interesting to note that although EB 3-8 has about half the gate length of EB 3-6 (and hence should have a smaller value of r_c), its imput impedance is significantly higher. It wouldn't seem that R_s is the culprit since it is already fairly low for EB 3-8 and it couldn't be much lower for EB 3-6. Rather, it seems that, because of the samller gate length, r_g has risen significantly, implying that the gate resistance is not as low as deduced previously

from the Al conductivity study (no control structures for ascertaining the Al conductivity were included in either of the Al evaporations for EB 2 or EB 3). It's hard to make any comparison in Table II between measurement and calculation since no two devices have the same L (and hence r_g and r_c) and R_s. In general, g_m compression and perhaps gate resistance seem to be responsible for the lack of better results from Run EB 3. At this point it was thought that the g_m compression could be dealt with by using an anodic cleaning before the gate deposition.

Run EB 4 (MBE wafer #115 with an n layer only) was not given an anodic cleaning before the gate Al deposition, and showed g_m compression. Run EB 5 (MBE wafer #117 with an n^+-on-n layer) was given the anodic etch, of course, and also showec g_m compression, discounting the previously held notion that the anodic etch would cure this problem. In spite of the complexities of the added n^+ layer, it was only with this layer that the unaccountably high values of g_m reported previously were seen, so an effort was made to fabricate a completed device having the n^+ layer.

Run EB 6 was done with MBE wafer #118. As with all the MBE wafers, the active layer was grown on an approximately one-micron thick buffer layer also grown by MBE. The active layer doping was estimated to be $3.5 \times 10^{17} \text{cm}^{-3}$ as deduced from the growth conditions. Devices were fabricated on this wafer using the anodic thinning process, and Au instead of Al was used as the gate metal. It was felt that perhaps the g_m compression was related to the Al, and maybe the use of Au might circumvent this problem.

The completed devices showed no g_m compression, and Fig. 20 shows a typical characteristic. Indeed, the g_m at zero

bias is quite high, being around 30-32 mmhos for the 150-micron wide devices. Two of the devices were rf tested in an amplifier circuit, giving the results shown in Table III.

TABLE III

8-GHz Performance for Run EB 6

Device	MAG (dB)	NF_m (dB)	G_a (dB)	L
EB 6-1	14.4	2.23	12.0	0.445
EB 6-5	14.2	2.2	12.2	0.305

It is interesting to note that although EB 6-5 has two-thirds the gate length of EB 6-1, its rf performance is virtually the same.

Fortunately, both these devices were able to be unbonded from the amplifier circuit and rebonded in the s-parameter jig. This enabled the results shown in Table IV to be obtained.

TABLE IV

Computed Noise Figure Performance at 8 GHz for Run EB 6

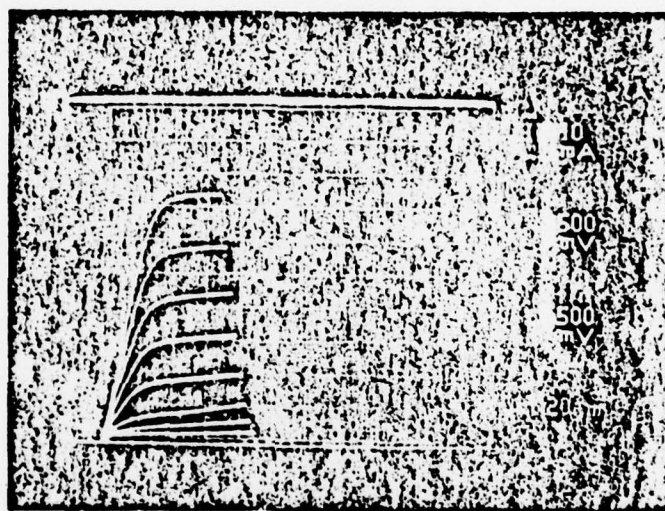| Device	r_{in} (ohm)	R_s (ohm)	NF_m (dB, BTL formula)
EB 6-1	18.15	3.1	2.14
EB 6-5	36.2	3.1	2.02

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Fig. 20. Drain characteristic for Run EB 6.

The computed values for the noise figure agree quite well with the measured values. Evidently the smaller gate length of EB 6-5 is offset by its higher input resistance, r_{in}. These values for r_{in} are for zero gate bias, but should not differ markedly from their values at the bias for minimum noise figure unless the channel resistance is significant. Since R_s is the same for both devices and since the channel resistance would seem to be smaller for the shorter gate length device, it appears that gate resistance is the culprit for the high input resistance. Preliminary tests seem to indicate that the gate metal conductivity is not at fault and that perhaps there is a high resistance interface layer between the gate metallization and the GaAs. This is presently being investigated.

Figure 21 gives a plot of I_d vs $\sqrt{\phi_B - V_g + I_d R_s}$ and shows a good linear characteristic almost to pinchoff, signifying a good active layer-buffer layer interface. The linearity also indicates constant doping across the channel. Assuming a channel doping of $3.5 \times 10^{17} cm^{-3}$, the slope gives a saturated drift velocity of $1.69 \times 10^7 cm/sec$ for EB 6-1 and $1.28 \times 10^7 cm/sec$ for EB 6-5. EB 6-5 has the shortest gate length and hence should have the most velocity overshoot, contrary to these results. Perhaps the doping varies across the wafer.

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Fig. 21. Saturated drift velocity determination for Run EB 6.
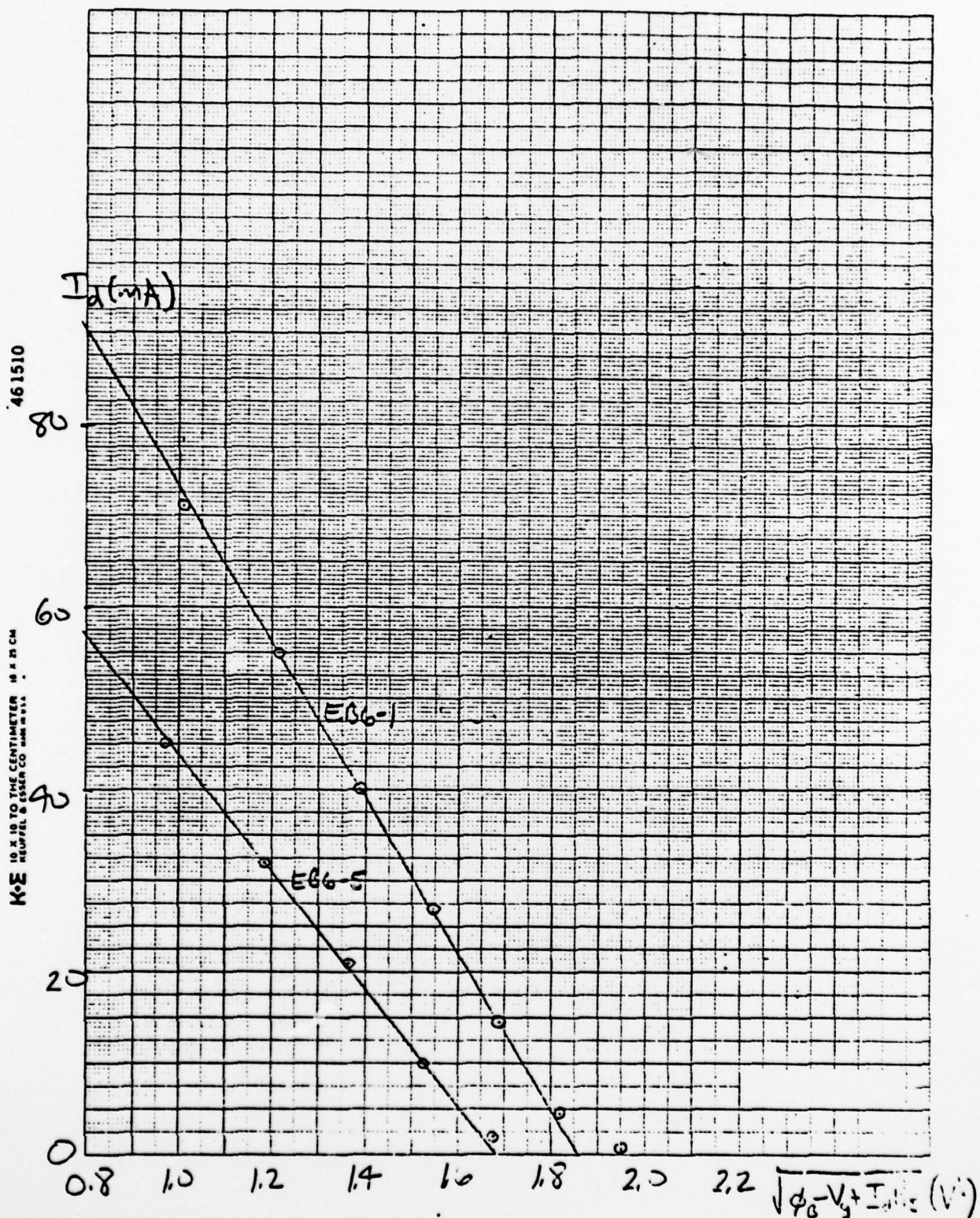
5.0 CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

GaAs FETs have been fabricated on MBE material using an anodic thinning procedure to remove the n^+ layer in the immediate vicinity of the gate. The gates are defined by electron-beam exposure and range in length from 0.15 to 0.45 microns. The use of the n^+ layer has resulted in the lowest source resistance (3.1 ohms) and the highest g_ms (30-32 mmhos) observed to date for 150-micron wide devices. The best rf data obtained at 8 GHz was a minimum noise figure of 2.2 dB with an associated gain of 12 dB for devices with gate lengths ranging from 0.3 to 0.45 microns.

In terms of device performance, it appears that the gate resistance may be the limiting factor. To ensure good liftoff, rather conservative thicknesses of gate metal have been deposited (3000 Å of Al for Run EB 3 and 2000 Å of Au for EB 6). An effort should be made to determine the maximum thickness of gate metal that can be reliably lifted. Even with the thicknesses used, the gate resistance should be much lower than the values inferred from the r_{in} measurements. Perhaps the gate profile is triangular rather than rectangular, and perhaps the conductivity is less than expected from previous trial runs (no control structures were included in the device gate depositions for conductivity determinations). As indicated by the increasing slope of the forward characteristic of the gates of Run EB 6 as they were turned on harder, there may be a high resistance interface layer between the gate metallization and the GaAs for that run. Perhaps the HCl etch to remove the anodic oxide should be replaced with a plasma etch to minimize possible contamination. New designs employing either multiple gate pads and/or a smaller device width should also be evaluated and implemented. Because of the

high g_ms achieved with the use of the n^+ layer, there may be no problem with off-the-chip driving capability with a narrower device.

In terms of yield, anodization damage to the ohmic contacts still occurs even with the use of Ti-W. The degree of damage varies from run to run, and was the yield limitation for Runs EB 3 and EB 6 which netted little more than the few devices tested. Shortening the delay between the Ti-W and SiO_2 depositions may solve this problem.

Another problem area is knowing the exact doping profile of the MBE wafers. This is necessary because the anodization without light stops when the pinch-off voltage equals the breakdown voltage, and further anodization must be done with light and a knowledge of how far to go. With light there is no natural stop action other than the applied voltage. The $\sim 10^{18} cm^{-3}$ doping of the n^+ layer makes profiling difficult because of leakage. Upon anodically thinning the $10^{18} cm^{-3}$ layer off, good profiles are still not obtained for the MBE active layer again because of leakage. This problem area should also be dealt with.

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